AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A delayed tap signal generating circuit comprising:

a first tap signal generating circuit adapted to receive a first clock signal and a second clock signal, which have a same frequency and a phase difference between them, adapted to receive offset information, and adapted to generate a first tap signal in response to the first and second clock signals and the offset information, wherein the first tap signal is delayed with respect to the first clock signal by a first delay corresponding to the offset information; and

a second tap signal generating circuit adapted to receive the first and second clock signals, adapted to receive the offset information, and adapted to generate a second tap signal in response to the first and second clock signals and the offset information, wherein the second tap signal is delayed with respect to the first clock signal by the first delay and a second delay added to the first delay, wherein the second delay corresponds to the offset information, and

wherein the first and second tap signals are generated by interpolating the first and second clock signals in response to the offset information.

2. (Original) The circuit of claim 1, wherein the first tap generating circuit comprises:

a first N-bit adder adapted to receive the offset information, convert the offset information into an N-bit digital signal, add a default signal to the N-bit digital signal, and output a first N-bit adder output signal;

a first digital/analog converting circuit adapted to receive the first N-bit adder output signal, convert the output signal of the first N-bit adder into a first analog signal, and output the first analog signal; and

a first interpolating circuit adapted to receive the first and second clock signals, interpolate the first and second clock signals in response to the first analog signal, and output the first tap signal.

3. (Original) The circuit of claim 2, wherein N is 6.

4. (Original) The circuit of claim 2, wherein the second tap signal generating circuit comprises:

a second N-bit adder adapted to receive the offset information, convert the offset information into a second N-bit digital signal, add the first N-bit adder output signal of the first N-bit adder to the second N-bit digital signal, and output a second N-bit adder output signal;

a second digital/analog converting circuit adapted to receive the second N-bit adder output signal, convert the second N-bit adder output signal into a second analog signal, and output the second analog signal;

a second interpolating circuit adapted to receive the first and second clock signals, interpolate the first and second clock signals in response to the second analog signal, and output the second tap signal.

5. (Original) The circuit of claim 4, where N is 6.

6. (Original) The circuit as claimed in claim 1, wherein the second delay is less than the phase difference between the first and second clock signals.

7. (Currently Amended) A delayed tap signal generating circuit adapted to receive a first clock signal and a second clock signal, which have the same frequency

and a phase difference between them, and adapted to generate a plurality of delayed tap signals, each of which has a delay less than the phase difference, the circuit comprising:

a second tap signal generating circuit adapted to generate a second tap signal in response to the first and second clock signals and an offset ~~information~~ value, wherein the second tap signal is delayed with respect to a first tap signal by a first delay corresponding to the offset ~~information~~ value;

a third tap signal generating circuit adapted to receive the first and second clock signals, and adapted to generate a third tap signal in response to the first and second clock signals and the offset ~~information~~ value, wherein third tap signal is delayed with respect to the first tap signal by the first delay and a second delay added to the first delay; and

a fourth tap signal generating circuit adapted to receive the first and second clock signals, and adapted to generate a fourth tap signal in response to the first and second clock signals and the offset ~~information~~ value, wherein the fourth tap signal is delayed with respect to the first tap signal by the first and second delays and a third delay added to the first and second delays,

wherein the first tap signal is the first clock signal, and

wherein the second, third, and fourth tap signals are generated by interpolating the first and second clock signals in response to the offset ~~information~~ value.

8. (Currently Amended) The circuit of claim 7, wherein the second tap signal generating circuit comprises:

a first N-bit adder adapted to receive the offset ~~information~~ value, convert the offset ~~information~~ value into a first N-bit digital signal, add a default signal to the first N-bit digital signal, and output a first N-bit adder output signal;

a first digital/analog converting circuit adapted to receive the a first N-bit adder output signal of the first N-bit adder, convert the a first N-bit adder output signal of the first N-bit adder into a first analog signal, and output the first analog signal; and

a first interpolating circuit adapted to receive the first and second clock signals, interpolate the first and second clock signals in response to the first analog signal, and output the first tap signal.

9. (Original) The circuit of claim 8, where N is 6.

10. (Currently Amended) The circuit of claim 8, wherein the third tap signal generating circuit comprises:

a second N-bit adder adapted to receive the offset ~~information~~ value, convert the offset ~~information~~ value into a second N-bit digital signal, add the first N-bit adder output signal of the first N-bit adder to the second N-bit digital signal, and output a second N-bit adder output signal;

a second digital/analog converting circuit adapted to receive the second N-bit adder output signal of the second N-bit adder, convert the second N-bit adder output signal of the second N-bit adder into a second analog signal, and output the second analog signal; and

a second interpolating circuit adapted to receive the first and second clock signals, interpolate the first and second clock signals in response to the second analog signal, and output the second tap signal.

11. (Original) The circuit of claim 10, where N is 6.

12. (Currently Amended) The circuit of claim 10, wherein the fourth tap signal generating circuit comprises:

a third N-bit adder adapted to receive the offset ~~information~~ value, convert the offset ~~information~~ value into a third N-bit digital signal, add the second N-bit adder output signal of the second N-bit adder to the third N-bit digital signal, and output a third N-bit adder output signal;

a third digital/analog converting circuit adapted to receive the third N-bit adder output signal of the third N-bit adder, convert the third N-bit adder output signal of the third N-bit adder into a third analog signal, and output the third analog signal; and

a third interpolating signal adapted to receive the first and second clock signals, interpolate the first and second clock signals in response to the third analog signal, and output the third tap signal.

13. (Original) The circuit as claimed in claim 12, wherein N is 6.

14. (Original) The circuit as claimed in claim 7, wherein the third delay is less than the phase difference between the first and second clock signals.

15. (Currently Amended) A method of generating delayed tap signals, the method comprising:

(a) receiving a first clock signal and a second clock signal, which have the same frequency and a phase difference between them, and receiving offset information, and generating a first tap signal in response to the first and second clock signals and the offset information, wherein the first tap signal is delayed with respect to the first clock signal by a first delay corresponding to the offset information; and

(b) receiving the first and second clock signals and the offset information and generating a second tap signal in response to the first and second clock signals and the offset information, wherein the second tap signal is delayed with respect to the first clock signal by the first delay and a second delay added to the first delay, wherein the second delay corresponds to the offset information, and

wherein the first and second tap signals are generated by interpolating the first and second clock signals in response to the offset information.

16. (Canceled)

17. (Currently Amended) The method as claimed in claim 15, wherein step (a) comprises:

(a1) receiving the offset information, converting the offset information into a first N-bit digital signal, adding a default signal to the first N-bit digital signal, and outputting a first N-bit adder output signal;

(a2) converting the first N-bit adder output signal from step (a1) into a first analog signal and outputting the first analog signal; and

(a3) receiving the first and second clock signals, interpolating the first and second clock signals in response to the first analog signal from step (a2), and outputting the first tap signal.

~~(b2) converting the second N-bit adder output signal from step (b1) into a second analog signal and outputting the second analog signal; and~~

~~(b3) receiving the first and second clock signals, interpolating the first and second clock signals in response to the second analog signal from step (b2), and outputting the second tap signal.~~

18. (Original) The method as claimed in claim 17, wherein step (b) comprises:

(b1) receiving the offset information, converting the offset information into a second N-bit digital signal, adding the first N-bit adder output signal from step (a1) to the second N-bit digital signal, and outputting a second N-bit adder output signal;

(b2) converting the second N-bit adder output signal from step (b1) into a second analog signal and outputting the second analog signal; and

(b3) receiving the first and second clock signals, interpolating the first and second clock signals in response to the second analog signal from step (b2), and outputting the second tap signal.

19. (Original) The method as claimed in claim 15, wherein the second delay is less than the phase difference between the first and second clock signals.

20. (Currently Amended) A method of generating delayed tap signals for receiving a first clock signal and a second clock signal, which have the same frequency and a phase difference between them, and generating a plurality of tap signals, each of which has a delay less than the phase difference, the method comprising:

generating a second tap signal in response to the first and second clock signals and an offset ~~information~~ value, wherein the second tap signal is delayed with respect to the first clock signal by a first delay corresponding to the offset ~~information~~ value;

receiving the first and second clock signals and generating a third tap signal in response to the first and second clock signals and the offset ~~information~~ value, wherein the third tap signal is delayed with respect to the first clock signal by the first delay and a second delay added to the first delay; and

receiving the first and second clock signals and generating a fourth tap signal in response to the first and second clock signals and the offset ~~information~~ value, wherein the fourth tap signal is delayed with respect to the first clock signal by the first and second delays, and a third delay added by the first and second delays,

wherein the first tap signal is the first clock signal, and

wherein the second, third, and fourth tap signals are generated by interpolating the first and second clock signals in response to the offset ~~information~~ value.

21. (New) The method of claim 20, further comprising receiving the offset value input by a user.